WHAT IS CLAIMED IS:

1. A method for generating a primary scrambling code and N secondary scrambling codes associated with the primary scrambling code for a mobile telecommunication system, the method comprising the steps of:

(a) generating a first m-sequence from a first shift register memory having a plurality of registers with values a_i (i = 0 to c-1 where c = the total number of the registers);

(b) generating a second m-sequence from a second shift register memory having a plurality of registers with values b_i (i = 0 to c-1 where c = the total number of the registers);

(c) adding the first m-sequence with the second m-sequence to generate the primary scrambling code;

(d) masking a_i (i = 0 to c-1) to produce a L^{th} secondary sequence which is a first m-sequence cyclically shifted L times, where $1 \leq L \leq N$; and

(e) adding the L^{th} secondary sequence with the second m-sequence to produce a L^{th} secondary scrambling code.

2. The method of claim 1, wherein the first and second m-sequences are generated based on a first generator polynomial and a second generator polynomial, respectively.

3. The method of claim 1, wherein the masking in step (d) is expressed by the following equation: $\sum(K^L{}_i \times a_i)$.

4. The method of claim 2, further comprising the step of cyclically shifting the first shift register memory.

5. The method of claim 4, wherein the step of cyclically shifting the first shift register memory comprises the steps of adding predetermined bits of the first shift register memory based on the first generator polynomial of the first m-sequence, right shifting the first shift register memory and inserting the value of the added predetermined bits into a_{c-1}.

6. The method of claim 5, wherein a_0 is added with a_7 to form a next a_{c-1}.

7. The method of claim 2, further comprising the step of cyclically shifting the second shift register memory.

8. The method of claim 7, wherein the step of cyclically shifting the second shift register memory comprises the steps of adding predetermined bits of the second shift register memory based on the second generator polynomial of the second m-sequence, right shifting the second shift register memory and inserting the value of the added predetermined bits into b_{c-1}.

9. The method of claim 8, wherein b_0 is added with b_5, b_7, and b_{10} to form a next b_{c-1}.

10. The method of claim 1, further comprising the step of delaying the L^{th} secondary scrambling code to produce a Q-channel component of the L^{th} secondary scrambling code, wherein the undelayed L^{th} secondary scrambling code is a I-channel component of the L^{th} secondary scrambling code.

11. A method for generating a primary scrambling code and N

secondary scrambling codes associated with the primary scrambling code for a mobile telecommunication system, the method comprising the steps of:

(a) generating a first m-sequence from a first shift register memory having a plurality of registers with values a_i (i = 0 to c-1 where c = the total number of registers);

(b) generating a second m-sequence from a second shift register memory having a plurality of registers with values b_i (i = 0 to c-1 where c = the total number of registers);

(c) adding the first m-sequence with the second m-sequence to generate the primary scrambling code;

(d) inputting a_i (i = 0 to c-1) into masking sections;

(e) masking a_i (i = 0 to c-1) in each of the masking sections to produce secondary sequences;

(f) adding each of the secondary sequences with the second m-sequence to produce the N secondary scrambling codes,

wherein a L^{th} secondary sequence is a first m-sequence cyclically shifted L times, where $1 \leq L \leq N$.

12. The method of claim 11, wherein the first and second m-sequences are generated based on a first generator polynomial and a second generator polynomial, respectively.

13. The method of claim 11, wherein the masking in step (e) is expressed by the following equation: $\sum (k^L_i \times a_i)$.

14. The method of claim 12, further comprising the step of cyclically shifting the first shift register memory.

15. The method of claim 14, wherein the step of cyclically shifting the first shift register memory comprises the steps of adding predetermined bits of the first shift register memory based on the first generator polynomial of the first m-sequence, right shifting the first shift register memory and inserting the value of the added predetermined bits into a_{c-1}.

16. The method of claim 15, wherein a_0 is added with a_7 to form a next a_{c-1}.

17. The method of claim 12, further comprising the step of cyclically shifting the second shift register memory.

18. The method of claim 17, wherein the step of cyclically shifting the second shift register memory comprises the steps of adding predetermined bits of the second shift register memory based on the second generator polynomial of the second m-sequence, right shifting the second shift register memory and inserting the value of the added predetermined bits into b_{c-1}.

19. The method of claim 18, wherein b_0 is added with b_5, b_7, and b_{10} to form a next b_{c-1}.

20. The method of claim 11, further comprising the step of delaying the each of the secondary scrambling codes to produce Q-channel components of the secondary scrambling codes, wherein the undelayed secondary scrambling codes are I-channel components of the secondary scrambling codes.

21. An apparatus for generating a primary scrambling code and secondary scrambling codes associated with the primary scrambling code for a

mobile telecommunication system, the apparatus comprising:

a first shift register memory for generating a first m-sequence, said first shift register memory having a plurality of registers with values a_i (i = 0 to c-1 where c = the total number of registers);

a second shift register memory for generating a second m-sequence, said second shift register memory having a plurality of registers with values b_i (i = 0 to c-1 where c = the total number of registers);

a primary adder for adding the first m-sequence with the second m-sequence to generate the primary scrambling code;

a plurality of masking sections for masking a_i (i = 0 to c-1) to produce secondary sequences; and

a plurality of secondary adders for adding the secondary sequences with the second m-sequence to produce the secondary scrambling codes,

wherein each of the masking sections cyclically shifts the first m-sequence by using a mask.

22. The apparatus of claim 21, wherein the first and second m-sequences are generated based on a first generator polynomial and a second generator polynomial, respectively.

23. The apparatus of claim 21, wherein the mask in each of the masking sections is expressed by the following equation: $\sum(k^{L_i} \times a_i)$.

24. The apparatus of claim 22, further comprising a first register adder for adding the bits of the first shift register memory, wherein the first shift register memory is cyclically shifted by adding predetermined bits of the first shift register memory in the first register adder based on the first generator

polynomial of the first m-sequence, right shifting the first shift register memory and inserting the output of the first register adder into a_{c-1}.

25. The apparatus of claim 24, wherein a_0 is added with a_7 to form a next a_{c-1}.

26. The apparatus of claim 24, further comprising a second register adder for adding the bits of the second shift register memory, wherein the second shift register memory is cyclically shifted by adding predetermined bits of the second shift register memory in the second register adder based on the second generator polynomial of the second m-sequence, right shifting the second shift register memory and inserting the output of the second register adder into a_{c-1}.

27. The apparatus of claim 26, wherein b_0 is added with b_5, b_7 and b_{10} to form a next b_{c-1}.

28. The apparatus of claim 21, further comprising a plurality of delay blocks for delaying the outputs of the primary adder and the secondary adders for producing Q channel components of the primary scrambling code and the secondary scrambling codes.

29. An apparatus for generating a primary scrambling code and a secondary scrambling code associated with the primary scrambling code for a mobile telecommunication system, the apparatus comprising:

a first shift register memory for generating a first m-sequence, said first shift register memory having a plurality of registers with values a_i (i = 0 to c-1 where c = the total number of registers);

a second shift register memory for generating a second m-sequence,

said second shift register memory having a plurality of registers with values b_i (i = 0 to c-1 where c = the total number of registers);

a primary adder for adding the first m-sequence with the second m-sequence to generate the primary scrambling code; and

a masking section for masking a_i (i = 0 to c-1) to produce a secondary sequence;

a secondary adder for adding the secondary sequence with the second m-sequence to produce the secondary scrambling code,

wherein the masking section cyclically shifts the first m-sequence by using a mask.

30. The apparatus of claim 29, further comprising a plurality of delay blocks for delaying the outputs of the primary adder and the secondary adder for producing Q channel components of the primary scrambling code and the secondary scrambling code.